CMOS Components for 802.11b Wireless LAN Applications

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***Abstracts** 2.4-GHz CMOS low noise amplifier, mixer, local oscillator buffer, differential power amplifier, and T/R switch for 802.11b Wireless Local Area Network (WLAN) applications have been implemented using MOS transistors. A single chip 2.4-GHz transceiver for WLAN with integrated power amplifier, switches, and other RF components will be possible in a 0.25-μm CMOS technology. More importantly, it appears that the CMOS solution will be highly competitive in the 2.4-GHz WLAN market.*

I. INTRODUCTION

Recent speed improvements of digital CMOS transistors have made it feasible to implement RF circuits operating at 1 GHz and above in CMOS technologies. As a low cost alternative, CMOS is becoming a contender for RF front-end IC applications [1],[2]. This paper discusses 2.4-GHz RF low noise amplifier (LNA) [3], mixer [3], T/R switch, and differential power amplifier for IEEE 802.11b standards. The performance of these components are comparable to those of SiGe solutions and suggest that a single chip 2.4-GHz transceiver for WLAN with integrated power amplifier, switches, and other RF components should be possible in a 0.25-μm CMOS technology.

II. CMOS LOW NOISE AMPLIFIER

Fig. 1 shows the schematic of the CMOS LNA. The circuit employs cascode topology for better isolation and reduced Miller effect. The input and output are matched to 50 Ω. Input matching is accomplished using an external transmission line and a shunt capacitor. Output is matched using a Pi matching network. The reason for this is, in a digital CMOS process, C_1 is implemented using a poly-to-n-well capacitor [4]. The poly-to-n-well capacitor has significant parasitic capacitance from its bottom plate. This makes the Pi matching network inevitable.

The circuit is housed in a 44 pin Micro Lead Frame (MLF) package with an exposed paddle. Fig. 2 shows a micro-photograph of the CMOS LNA. The actual die size of the CMOS LNA is 1100 μm X 1000 μm.

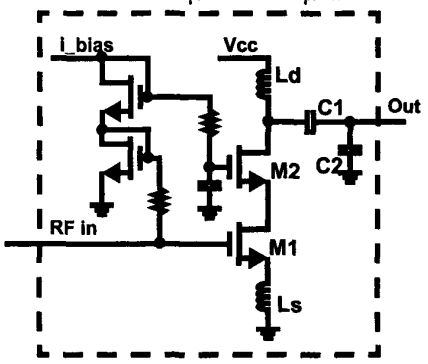

Fig. 1, A schematic of CMOS LNA.

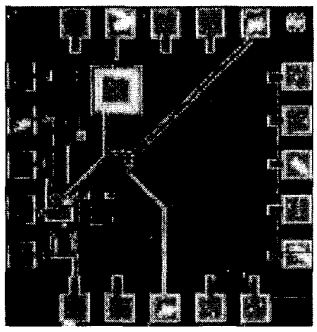

Fig. 2, A micro-photograph of the CMOS LNA.

Table 1 lists the measured results of CMOS and SiGe LNA's implemented in a 0.5-μm BiCMOS process with npn bipolar transistors with an f_T of 50 GHz. The SiGe LNA has the same circuit topology and was measured on essentially the same board and in the same package. Most of the CMOS specs are close to or exceed those of the SiGe ones, and this is achieved at the cost of an additional 1.1 mA, or roughly 15% increase in bias current. The bias current of CMOS LNA was chosen to match the SiGe specs. Compared to other CMOS and SiGe LNA's [5],[6], the

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noise figure of these two are on the high end. A preliminary study suggests that this is due to the fact that the mutual inductances introduced from packaging and bond wires can significantly increase the N.F. of the LNA. The 44 pin MLF package used in this study has a small footprint and the neighboring pins are much closer than in other packages, resulting in a larger mutual inductance between pins and bond wires.

The IIP_3 of CMOS LNA is 4.8 dB and 4.2 dB higher than that for the SiGe one. This is expected since MOSFET's are generally more linear than BJT's under the similar bias condition. Lastly, the circuit can also be made to operate at the same supply current as the SiGe one. This will result in a 0.05 dB increase in noise figure and 0.5 dB decrease in gain, which are small differences.

Table 1: CMOS and SiGe LNA Comparison

f_0 = 2.45 GHz	CMOS LNA	SiGe LNA
50-ohm NF	2.88 dB	2.86 dB
Bias Current	8.1 mA	7.0 mA
Transducer Gain	15.1 dB	15.9 dB
S_{11}	-14.2 dB	-12.7 dB
S_{22}	-20.2 dB	-16.0 dB
S_{12}	< -34	< -30
IIP_3	2.2 dBm	-2.6 dBm

III. CMOS MIXER

Fig. 3 shows the schematic of CMOS Rx mixer. The mixer is a Gilbert type double balanced active mixer. The RF input is matched to 50 Ω using the same kind of matching network used for the LNA input matching. The IF outputs are matched to a 200-Ω differential load through an off-chip matching network shown in Fig. 6

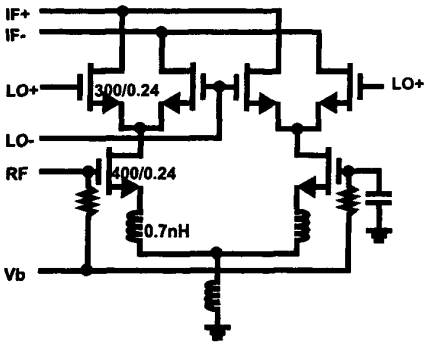

Fig. 3, A schematic of the CMOS Rx Mixer

The LO differential signals are generated on chip using an LO converter/buffer/driver. Fig. 7 shows the CMOS converter/buffer/driver schematic. The output of the off-chip VCO is single ended and is converted to differential using an on-chip converter. The differential signal is then buffered by source followers and amplified to drive the mixer switching core. The circuit implementations of the SiGe converter/ buffer/driver are similar. In the CMOS converter/buffer, bias current is 5 mA and the driver utilizes an inductive load in order to deliver a larger amplitude LO to the mixer switching core.

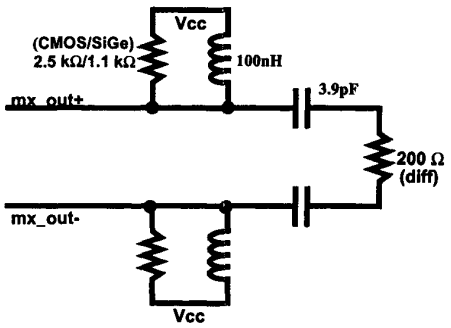

Fig. 4, Rx mixer output matching network

Table 2 lists the measurement results of the CMOS mixer and a SiGe mixer once again tested on the same board and package. The CMOS mixer exhibits approximately the same gain and return losses. The SSB noise figure is 1.5 dB higher for the CMOS mixer. An explanation of this is, for the CMOS mixer, with sinusoidal LO signals, the switching core transistors are simultaneously on for a larger portion of a period than its SiGe bipolar counterpart. Even though for the CMOS mixer, the LO signal is designed to have twice the magnitude as that of the bipolar one, namely, 0.3 V versus 0.15 V, the amount of time when both switching transistors are on is still larger than that in the bipolar differential pair switches.

Table 2: CMOS and SiGe Rx Mixer Comparison

LO=2.1GHz	CMOS Mixer	SiGe Mixer
Power Gain	8.0 dB	8.1 dB
SSB NF	10.5 dB	9.0 dB
Core Bias Current	12 mA	10 mA
Buffer/Driver Bias	8 mA	5 mA
RF Input S_{11}	-12.4 dB	-20.5 dB
LO Input S_{11}	-12.3 dB	-10.7 dB
IIP_3	3.0 dBm	6.2 dBm
LO to IF feedthru	-32 dB	-40 dB

IIP_3 of the CMOS mixer is around 3 dB lower than that for the SiGe mixer. There are two reasons for this. First, in the SiGe mixer, the inductive degeneration for the RF transistors (M1 & M2) is 2nH, which is much higher than 0.7 nH used in the CMOS mixer. This inductor was kept lower to achieve

the same gain in the CMOS mixer without increasing the power consumption. Second, the larger LO signal for the CMOS mixer introduces a larger signal at 2 X LO frequency (2-LO signal) on the drain node of the RF transistors. This 2-LO signal is coupled to the gates of RF transistors through C_{gd} of the MOS transistors and is known to degrade the linearity. Despite the slightly inferior noise figure and IIP_3, the CMOS mixer still satisfies the Rx mixer specifications for the PRISM II system.

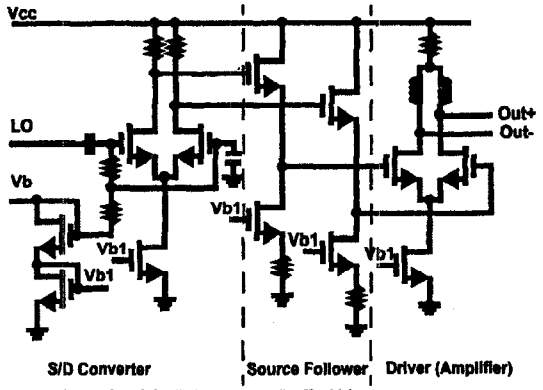

Fig. 5, A schematic of the LO converter/buffer/driver.

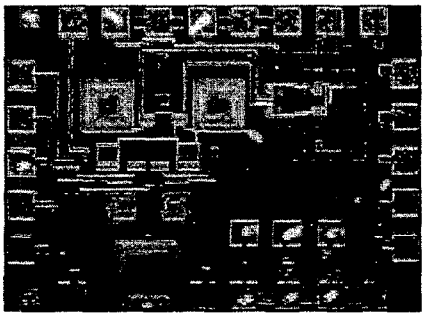

Fig. 6, A micro-photograph of the CMOS Rx mixer.

The CMOS mixer core consumes only 20% more power than the SiGe mixer. However, if the LO converter/buffer/driver power consumption is included, this number goes up to 33%. Fig. 9 shows a micro-photograph of the CMOS mixer. The CMOS mixer is also a stand alone circuit. Same as in the LNA case, for the CMOS mixer, the pad size and spacing, as well as the pad arrangement, function and orientation are kept the same as those of the SiGe mixer. The die size of the CMOS mixer is 1500 μm X 1100 μm.

IV. SPDT SWITCH

Another key blocks in a WLAN system are antenna diversity and T/R switches. A switch with P_{1dB} point of 20.6 dBm has been implemented using 0.35-μm high voltage transistors of a 0.18-μm CMOS process. In order to deliver higher than 20 dBm of power to a 50-Ω antenna, the peak-to-peak voltage swing at the antenna must be about 6.3 V. This voltage swing is too high to guarantee long term reliability. A technique to overcome these limitations is using matching networks to transform down 50-Ω source/load impedances (Z_S and Z_L) to ~20 Ω. Transforming the impedance substantially below 20 Ω is not advisable because this will significantly degrade insertion loss (IL).

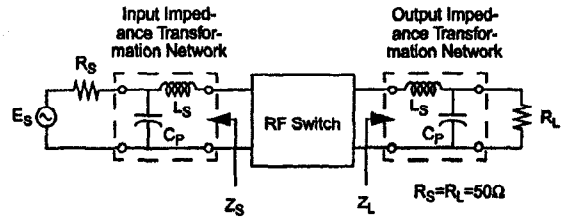

Fig. 7, Block diagram of an RF switch with impedance transformation networks.

Fig. 7 shows the block diagram of the switch including impedance transformation networks. The switch is represented as a two port network. R_S and R_L are 50-Ω source and load impedances, and Z_S and Z_L are the transformed source and load impedances seen by the switch. L_S's and C_P's are components for impedance transformation. L_S's are implemented using a combination of the bond wire and package lead inductances.

Figs. 8 and 9 are a circuit schematic and a micro-photographs of the switch. The die area is 531 x 531 μm^2. Substrate contacts have been carefully laid out to ensure the impact of p^- substrates on IL is reduced. Approximately, 63% of the die area is occupied by substrate contacts to reduce the substrate resistances.

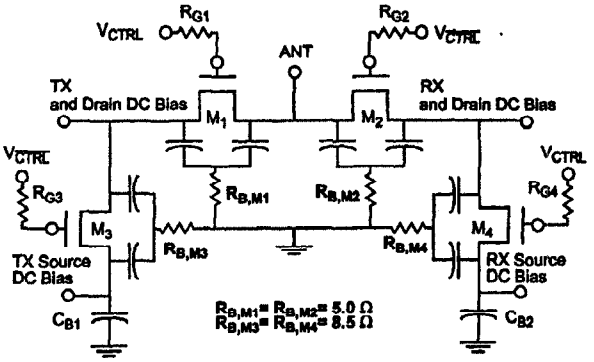

Fig. 8, Circuit schematic of an SPDT T/R switch including key substrate resistances. (R_B: substrate resistance)

Fig. 10 shows the measured IL and isolation for the switch. The measured IL is less than 1.2 dB for frequencies between 2.32 to 2.60 GHz. At 2.49 GHz, the measured IL is 1.1 dB and isolation is 20.6 dB. P_{1dB} is 20.6 dBm and IP_{1dB} is 23.0 dBm. The measured IP_3 is 29.8 dBm and IIP_3 is 31.1 dBm. The switches have been stressed at 20-dBm available power from the source (P_{AVS}) with the output open and also been stressed at 26 dBm P_{AVS} with a 50-Ω output load, and no degradation of the switch characteristics has been

observed. These suggest that the switch can operate all the way to P_{1dB} without being limited by a reliability problem.

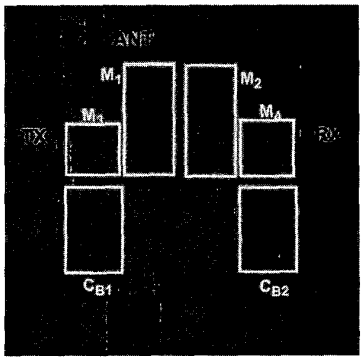

Fig. 9, Micro-photograph of the 0.35-μm SPDT switch.

In addition, the same transistor core was used to demonstrate a 900-MHz switch with 23 dBm P_{1dB} once again using impedance transformation. This suggests that it is possible to implement a 2.4 GHz T/R switch with P_{1dB} at 23 dBm. Incidentally, this level of switch performance cannot be attained using the MOS transistors in the 0.5-μm SiGe BiCMOS process. To integrate switches using a BiCMOS process, a more advanced BiCMOS process at higher cost must be utilized.

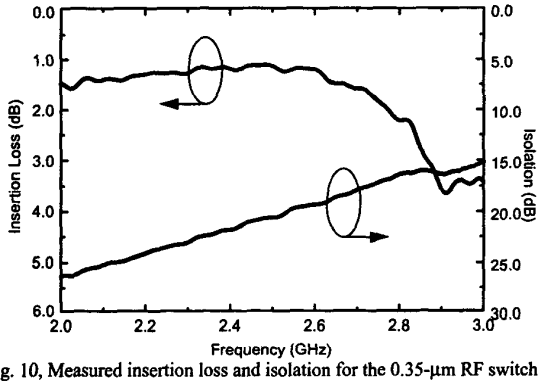

Fig. 10, Measured insertion loss and isolation for the 0.35-μm RF switch with 2.4-GHz impedance transformation networks.

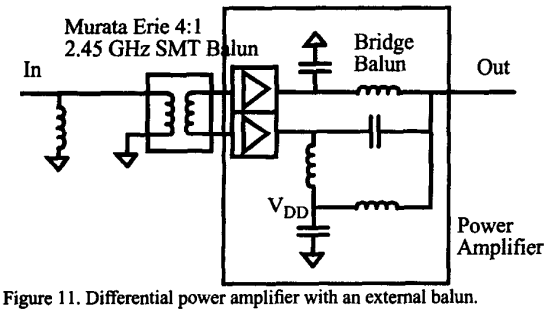

Figure 11. Differential power amplifier with an external balun.

V. POWER AMPLIFIER

Figure 11 shows a 2.4-GHz power amplifier implemented using a 0.25-μm CMOS process with 0.35-μm high voltage transistors. The amplifier is fully differential and the output is converted to single ended using an external balun. The power amplifier exhibits P_{1dB} compression point of 23 dBm. The output power spectrum under modulation is shown in Figure 12. At 20 dBm output power, the power added efficiency (PAE) is 17%, and the amplifier is compliant to the 802.11b side-lobe specifications at 11Mbps. This compares favorably to the PAE of 11% at 18 dBm for the SiGe power amplifier in the PRISM II chip set.

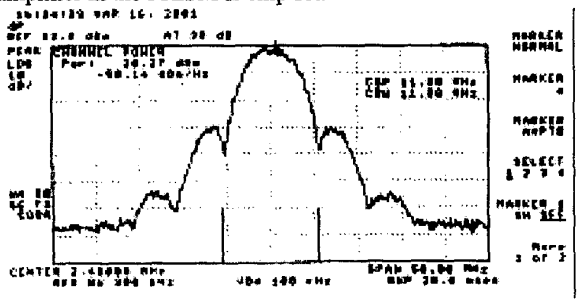

Figure 12. At 20 dBm output, power, the power added efficiency (PAE) is 17%, and the amplifier is compliant to the 802.11b side-lobe specifications

VI. CONCLUSIONS

A single chip 2.4-GHz transceiver for WLAN with integrated power amplifier, switches, and other RF components appears to be possible in a 0.25-μm CMOS technology with 0.35-μm 3.3-V transistors. The CMOS transceiver circuits consume 20 to 30% more power compared to those of the SiGe circuits, while the CMOS PA is more power efficient than the existing SiGe solution. It appears that CMOS solutions will be highly competitive in the 2.4-GHz WLAN market.

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